CLAIMS

What is claimed is:

1. A method for clock generation and distribution in an emulation system comprising:

generating a derived clock signal from a look up table, wherein an index to the look up table is generated by counting cycles of a base clock signal;

stopping emulation by stopping the base clock signal, wherein the index to the look up table is stopped at a stopping point in the derived clock cycle and the derived clock signal does not continue to a subsequent transition before stopping; and

resuming emulation by resuming the base clock signal, wherein the derived clock signal is resumed at the stopping point in the derived clock signal cycle.

2. The method of claim 1, wherein the step of generating a derived clock signal further comprises:

accessing an entry in a look up table having an address corresponding to the number of intermediate clock signals that have been counted; and

outputting a signal level in response to the entry accessed.

3. An emulation system comprising:

a plurality of emulation boards each having hardware to emulate one or more circuit designs;

means for interconnecting the plurality of emulation boards;

a clock generation circuit comprising

a base clock generation circuit that generates a base clock signal of a first frequency, and

a derived clock generation circuit having

a frequency divider circuit coupled to receive the base clock signal,

a counter circuit coupled to receive an output of the frequency divider circuit, and

a look up table coupled to receive an output of the counter circuit, wherein the output of the counter circuit is used to index entries in the look up table, and further wherein the entries in the look up table indicate a signal level for a derived clock signal generated by the clock generation circuitry.

4. The emulation system of claim 3, further comprising a plurality of clock generation circuits coupled in parallel to generate a plurality of derived clock signals.

5. The emulation system of claim 4, wherein the plurality of clock generation circuits each further comprise a selection circuit comprising a multiplexor coupled to receive the base clock signal and to receive an external clock signal from an external source, the multiplexor having an output coupled to the frequency divider circuit, wherein a select input of the multiplexor is provided by the external source.

6. The emulation system of claim 5, wherein the plurality of clock generation circuits each further comprise a frequency multiplier circuit that multiplies the external clock signal and provides a multiplied external clock signal to the multiplexor.

7. The emulation system of claim 3, wherein the clock signal is distributed to the plurality of emulation boards.

8. An apparatus for generating clock signals in an emulation system comprising:

means for generating a derived clock signal from a look up table, wherein an index to the look up table is generated by counting cycles of a base clock signal;

means for stopping emulation by stopping the base clock signal, wherein the index to the look up table is stopped at a stopping point in the derived clock cycle and the derived clock signal does not continue to a subsequent transition before stopping; and

means for resuming emulation by resuming the base clock signal, wherein the derived clock signal is resumed at the stopping point in the derived clock signal cycle.

9. The apparatus of claim 8, wherein the means for generating a derived clock signal further comprises:

means for accessing an entry in a look up table having an address corresponding to the number of intermediate clock signals that have been counted; and

means for outputting a signal level in response to the entry accessed.